Patent Claims

1.   A method for automatic identification of the clock
frequency of a system clock (15) for the configuration
of a peripheral device (12), having the following
steps:

generation of a secondary clock (16) at a predetermined
clock frequency;

application of the system clock (15) and of the
secondary clock (16) to a host (10);

application of the system clock (15) and of the
secondary clock (16) to the peripheral device (12);

determination of the clock frequency of the system
clock (15) in the peripheral device (12) by means of
the secondary clock (16); and

configuration of the peripheral device (12) using the
determined system clock (15).

2.   The method as claimed in claim 1,
wherein
the clock frequency of the system clock (15) is
determined by counting a number of edge changes of the
system clock (15) within a predetermined number of
periods of the secondary clock (16).

3.   The method as claimed in claim 1 or 2,
wherein,
during the configuration of the peripheral device (12),
the identical interface transmission rate is set for a
first interface (11) of the host (10) and for a second
interface (13) of the peripheral device (12) as a
function of the clock frequency of the determined
system clock (15).

4.   The method as claimed in claim 3,
wherein
the interface transmission rate is set to an interface
transmission rate which is defined by the standard of
the interfaces (11, 13).

5.   The method as claimed in one of the preceding
claims,
wherein,
after an initialization phase, the system clock (15)
can be changed by the main device (10) with a system
clock (which is then new) of the peripheral device (12)
being signaled exactly via interfaces (11, 13).

6.   The method as claimed in one of the preceding
claims,
wherein
tolerances of both the system clock (15) and of the
secondary clock (16) are taken into account in the
determination of the clock frequency of the system
clock (15) by the peripheral device (12).

7.   The method as claimed in one of the preceding
claims,
wherein
the transmission rate of the data transmission (14)
between a first interface (11) and a second interface
(13) is dependent on the clock frequency of the system
clock (15).

8.   The method as claimed in one of the preceding
claims,
wherein
the clock frequency of the system clock (15) is
variable at predetermined clock frequencies and is
determined by the host (10) after an initialization
phase.

9.   The method as claimed in claim 8,

wherein

the clock frequency of the system clock (15), which is

5   determined automatically by the peripheral device (12),

has discrete clock frequencies which are compared in

the   peripheral   device   (12)   with   discrete   clock

frequencies that are stored in a table, in order to use

the tabular value of the clock frequency as the current

10   clock frequency of the system clock (15).

10.   The method as claimed in one of the preceding

claims,

wherein

15   a PLL circuit (17) in the peripheral device (12)

generates a constant clock frequency (18) from the

clock frequency of the system clock (15), which clock

frequency (18) is supplied to a second interface (13)

and/or to a processing device (19), such as a

20   processor, controller or memory.

11.   The method as claimed in one of the preceding

claims,

wherein

25   the peripheral device (12) is a Bluetooth module, and

is configured for the system clock of a mobile radio

device, for example a cellular telephone.